A-008312 Duplicate Interrupt Possible with Edge-Triggered Interrupts

Errata Description

Title:

Duplicate edge-triggered interrupt after priority re-arbitration.

Description:

There is an occurrence of duplicate interrupt when an edge-triggered interrupt higher in priority comes closely to any other enabled interrupts. The following is the sequence of events that leads to the duplicate edge-triggered interrupt::

- 1. An active interrupt is waiting for acknowledgement
- 2. An edge-triggered interrupt of higher priority triggers closely to the lower priority interrupt just when it is acknowledged
- 3. The higher priority edge-triggered interrupt supersedes and fires a new interrupt to the core
- 4. The core acknowledges the higher priority interrupt without clearing the pending state and finishes the interrupt service routine with EOI
- 5. A duplicate of the higher priority edge-triggered interrupt is triggered because of the uncleared pending state

Impact:

Enabling any edge-triggered interrupts higher in priority than other enabled interrupts may lead to the duplicate edge-triggered interrupt. This includes edge-triggered IRQs, global timers and IPI.

Workaround:

Chose one of the following workarounds based on the interrupt type:

- Configure the higher priority interrupts as level-sensitive only
  a. In case of IRQs this can be configured in the Vector/Priority Register.
  b. It is not an option for global timers or IPI.
- Any enabled edge-triggered interrupts must be no higher in priority than the other enabled interrupts.

Resolution:

No plan to fix


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